

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-296245  
(43)Date of publication of application : 29.10.1999

(51)Int.Cl. G05F 3/26  
G05F 3/24  
H02J 1/00  
H03F 1/00  
H03K 17/04  
H03K 17/687

(21)Application number : 10-103004 (71)Applicant : NEC CORP  
(22)Date of filing : 14.04.1998 (72)Inventor : KOBAYASHI KATSUTARO

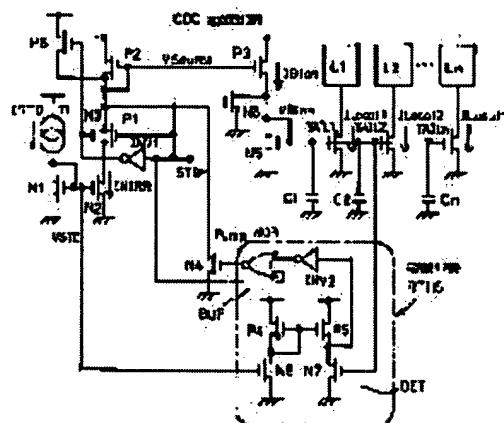
## (54) SEMICONDUCTOR CIRCUIT

(57) Abstract:

**PROBLEM TO BE SOLVED:** To set up the biasing time of a semiconductor circuit for temporarily increasing current supply and biasing it to an optimum value independently of power supply voltage, ambient temperature, manufacturing characteristics and parasitic capacity by supplying an operation bias current to load circuits, stopping current supply in a stand-by state and shortening restoration time when restoring an operation state from the stand-by state.

**SOLUTION:** At the time of restoration to an operation state, current supply to a current driving circuit(CDC) for inputting a signal to a restoring transistor(TR) N4 and supplying a bias current to load circuits L1 to Ln is increased. A restoration speeding-up circuit RTHS for inputting the signal to the TR N4 is constituted as a current detection circuit, wherein the bias current supplied to the load circuits L1 to Ln is compared with a constant current and signal input to the TR N4 is controlled based on the compared result to determine supply time of the bias current.

Consequently adjustment of a delay due to power supply voltage, ambient temperature, characteristic deviations of manufacture, a difference of parasitic capacity, etc., is not required, the bias time can be held at a proper time without being shortened or excessively extended and restoration time from the stand-by mode can be shortened.



## LEGAL STATUS

[Date of request for examination] 14.04.1998

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

[application converted registration]

[Date of final disposal for application]

[Patent number] 3147079

[Date of registration] 12.01.2001

[Number of appeal against examiner's decision of  
rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office